

## WHAT IS CLAIMED IS:

- 1        1.        A voltage controlled oscillator (VCO) having a VCO output signal with  
2        selectable frequency ranges comprising:  
3                M inverting circuits coupled in series forming M+1 nodes N(1) to N(M+1),  
4        wherein M is an odd integer number greater than three;  
5                M voltage controlled feedforward inverting (VCFF) circuits, each VCFF(J)  
6        having a control voltage input, a signal input I(J) coupled to a corresponding node  
7        N(J), where J is a number (1 to M), and a signal output X(J), the first number (M-2K)  
8        of the signal outputs X(1) to X(M-2K) are coupled to corresponding nodes N(4) to  
9        N(M-2K+3);  
10               first circuitry for selectively coupling a first feedback signal selected from  
11               signals on K of first candidate nodes (N(M+1) to N(M-2K+3)), to node N(1), wherein  
12               K is an integer number greater than or equal to two and less than or equal to (M-5), in  
13               response to the one or more latched select signals, thereby generating the VCO output  
14               signal;  
15               second circuitry for selectively coupling a second feedback signal from  
16               signals on K second candidate outputs X(M-1) to X(M-2K+1) to node N(2) in  
17               response to the one or more latched select signals; and  
18               third circuitry for selectively coupling a third feedback signal from signals on  
19               K third candidate outputs X(M) to X(M-2K+2) to node N(3) in response to the one or  
20               more latched select signals.
- 1        2.        The VCO of claim 1, wherein the one or more latched select signals are  
2        generated by latching asynchronous select signals when the first feedback signal  
3        coupled to node N(1) from a presently selected node N(Pr) from nodes N(M+1) to  
4        N(M-2K+3) setting of a present frequency range of the VCO has the same logic state

5 as a signal on a next selected node  $N(P_n)$  setting a next frequency range, thereby  
6 assuring switching from the present frequency range to the next frequency range of  
7 the VCO occurs glitch free.

1 3. The VCO of claim 1, wherein the number of candidate outputs  $K$  is limited by  
2 the requirement that all of the  $K$  first candidate outputs have the same logic state for a  
3 time period necessary to generate a new latched select signal and to switch between a  
4 present and a next candidate output.

1 4. The VCO of claim 1, wherein the VCO output signal is generated at node  
2  $N(1)$  or node  $N(M+1)$ .

1 5. The VCO of claim 1, wherein the one or more latched select signals are  
2 generated by latching asynchronous select signals on a state of a signal selected from  
3 signals on one of the  $K$  first candidate nodes  $N(M+1)$  to  $N(M-2K+3)$ .

1        6.        A phase locked loop circuit for generating an output clock signal with a  
2        selectable frequency range and a frequency that is a multiple number  $N$  times the  
3        frequency of a reference clock signal comprising:

4                a voltage controlled oscillator (VCO) generating the output clock signal with a  
5        frequency range set by one or more frequency range select signals, a frequency  
6        divider for frequency dividing the output clock signal by  $N$  generating a frequency  
7        divided clock signal, a phase frequency detector for comparing the frequency divided  
8        clock signal to the reference clock signal and generating a phase/frequency error  
9        signal, circuitry for converting the phase/frequency error signal to the control voltage,  
10       the VCO having  $M$  of inverting circuits (IVC) coupled in series forming  $M+1$  nodes  
11        $N(1)$  to  $N(M+1)$ , wherein  $M$  is an odd integer number including greater than three,  
12       the VCO having:

13                 $M$  voltage controlled feedforward inverting (VCFF) circuits, each VCFF( $J$ )  
14       having a control voltage input, a signal input  $I(J)$  coupled to a corresponding node  
15        $N(J)$ , where  $J$  is a number (1 to  $M$ ), and a signal output  $X(J)$ , the first number ( $M-2K$ )  
16       of the signal outputs  $X(1)$  to  $X(M-2K)$  are coupled to corresponding nodes  $N(4)$  to  
17        $N(M-2K+3)$ ;

18                first circuitry for selectively coupling a first feedback signal selected from  
19       signals on  $K$  of first candidate nodes ( $N(M+1)$  to  $N(M-2K+3)$ ), to node  $N(1)$ , wherein  
20        $K$  is an integer number greater than or equal to two and less than or equal to ( $M-5$ ), in  
21       response to the one or more latched select signals, thereby generating the VCO output  
22       signal;

23                second circuitry for selectively coupling a second feedback signal from  
24       signals on  $K$  second candidate outputs  $X(M-1)$  to  $X(M-2K+1)$  to node  $N(2)$  in  
25       response to the one or more latched select signals; and

26           third circuitry for selectively coupling a third feedback signal from signals on  
27   K third candidate outputs  $X(M)$  to  $X(M-2K+2)$  to node  $N(3)$  in response to the one or  
28   more latched select signals.

1       7.     The phase locked loop circuit of claim 6, wherein the one or more latched  
2   select signals are generated by latching asynchronous select signals when the first  
3   feedback signal coupled to node  $N(1)$  from a presently selected node  $N(P_r)$  from  
4   nodes  $N(M+1)$  to  $N(M-2K+3)$  setting of a present frequency range of the VCO has  
5   the same logic state as a signal on a next selected node  $N(P_n)$  setting a next frequency  
6   range, thereby assuring switching from the present frequency range to the next  
7   frequency range of the VCO occurs glitch free.

1       8.     The phase locked loop circuit of claim 6, wherein the number of candidate  
2   outputs K is limited by the requirement that all of the K first candidate outputs have  
3   the same logic state for a time period necessary to generate a new latched select  
4   signal and to switch between a present and a next candidate output.

1       9.     The phase locked loop circuit of claim 6, wherein the output clock signal is  
2   generated at node  $N(1)$  or node  $N(M+1)$ .

1       10.    The phase locked loop circuit of claim 6, wherein the one or more latched  
2   select signals are generated by latching asynchronous select signals on a state of a  
3   signal selected from signals on one of the K first candidate nodes  $N(M+1)$  to  $N(M-$   
4    $2K+3)$ .

1        11.     A data processing system comprising:  
2                a central processing unit (CPU) clocked by a CPU clock signal;  
3                a random access memory (RAM);  
4                a read only memory (ROM);  
5                an I/O adapter;  
6                a bus system coupling said CPU to said ROM, said communications adapter,  
7                said I/O adapter, and said RAM, wherein the CPU clock signal is generated by phase  
8                locked loop circuitry with a frequency a multiple number N times the frequency of a  
9                reference clock signal comprising:  
10               a voltage controlled oscillator (VCO) generating the output clock signal with a  
11               frequency range set by one or more frequency range select signals, a frequency  
12               divider for frequency dividing the output clock signal by N generating a frequency  
13               divided clock signal, a phase frequency detector for comparing the frequency divided  
14               clock signal to the reference clock signal and generating a phase/frequency error  
15               signal, circuitry for converting the phase/frequency error signal to the control voltage,  
16               the VCO having M of inverting circuits (IVC) coupled in series forming M+1 nodes  
17               N(1) to N(M+1), wherein M is an odd integer number including greater than three,  
18               the VCO having;  
19               M voltage controlled feedforward inverting (VCFF) circuits, each VCFF(J)  
20               having a control voltage input, a signal input I(J) coupled to a corresponding node  
21               N(J), where J is a number (1 to M), and a signal output X(J), the first number (M-2K)  
22               of the signal outputs X(1) to X(M-2K) are coupled to corresponding nodes N(4) to  
23               N(M-2K+3);  
24               first circuitry for selectively coupling a first feedback signal selected from  
25               signals on K of first candidate nodes (N(M+1) to N(M-2K+3)), to node N(1), wherein  
26               K is an integer number greater than or equal to two and less than or equal to (M-5), in

27 response to the one or more latched select signals, thereby generating the VCO output  
28 signal;

29 second circuitry for selectively coupling a second feedback signal from  
30 signals on K second candidate outputs  $X(M-1)$  to  $X(M-2K+1)$  to node N(2) in  
31 response to the one or more latched select signals; and

32 third circuitry for selectively coupling a third feedback signal from signals on  
33 K third candidate outputs  $X(M)$  to  $X(M-2K+2)$  to node N(3) in response to the one or  
34 more latched select signals.

1 12. The data processing system of claim 11, wherein the one or more latched  
2 select signals are generated by latching asynchronous select signals when the first  
3 feedback signal coupled to node N(1) from a presently selected node N(Pr) from  
4 nodes N(M+1) to N(M-2K+3) setting of a present frequency range of the VCO has  
5 the same logic state as a signal on a next selected node N(Pn) setting a next frequency  
6 range, thereby assuring switching from the present frequency range to the next  
7 frequency range of the VCO occurs glitch free.

1 13. The data processing system of claim 11, wherein the number of candidate  
2 outputs K is limited by the requirement that all of the K first candidate outputs have  
3 the same logic state for a time period necessary to generate a new latched select  
4 signal and to switch between a present and a next candidate output.

1 14. The data processing system of claim 11, wherein the output clock signal is  
2 generated at node N(1) or node N(M+1).

1 15. The data processing system of claim 11, wherein the one or more latched  
2 select signals are generated by latching asynchronous select signals on a state of a

3        signal selected from signals on one of the K first candidate nodes  $N(M+1)$  to  $N(M-$   
4         $2K+3)$ .  
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